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1 Limits of control flow on parallelism   ◼
Monica S. Lam, Robert P. Wilson
April 1992 **ACM SIGARCH Computer Architecture News , Proceedings of the 19th annual international symposium on Computer architecture**, Volume 20 Issue 2

Full text available: 📄 pdf(1.30 MB)   Additional Information: full citation, abstract, references, citings, index terms

This paper discusses three techniques useful in relaxing the constraints imposed by control flow on parallelism: control dependence analysis, executing multiple flows of control simultaneously, and speculative execution. We evaluate these techniques by using trace simulations to find the limits of parallelism for machines that employ different combinations of these techniques. We have three major results. First, local regions of code have limited parallelism, and control dependence analysis ...

2 Is SC + ILP = RC?   ◼
Chris Gniady, Babak Falsafi, T. N. Vijaykumar
May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture**, Volume 27 Issue 2

Full text available: 📄 pdf(94.82 KB) 📑 Additional Information: full citation, abstract, references, citings, index terms
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Sequential consistency (SC) is the simplest programming interface for shared-memory systems but imposes program order among all memory operations, possibly precluding high performance implementations. Release consistency (RC), however, enables the highest performance implementations but puts the burden on the programmer to specify which memory operations need to be atomic and in program order. This paper shows, for the first time, that SC implementations can perform as well as RC implementations ...

3 Instruction Scheduling for Dynamic Hardware Configurations   ◼
Elena Moscu Panainte, Koen Bertels, Stamatis Vassiliadis
March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1**

Full text available: 📄 pdf(165.23 KB)   Additional Information: full citation, abstract

Although the huge reconfiguration latency of the available FPGA platforms is a well-known shortcoming of the current FCCMs, little research in instruction scheduling has been undertaken to eliminate or diminish its negative influence on performance. In this paper, we introduce an instruction scheduling algorithm that minimizes the number of executed

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